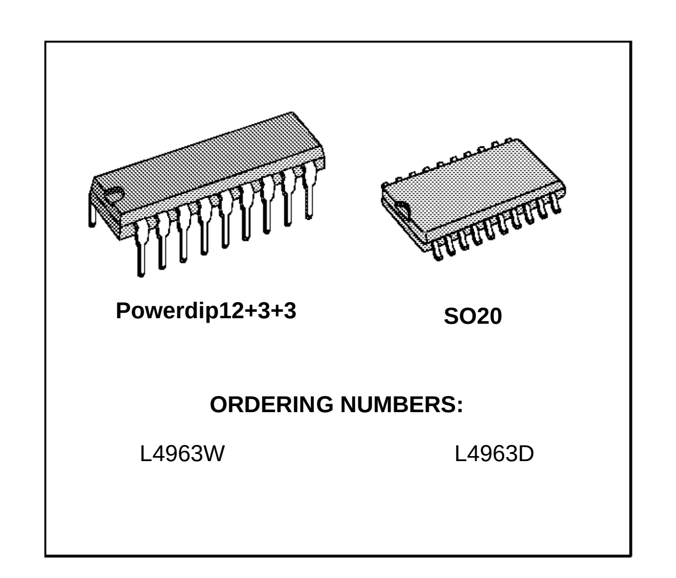


L4963
L4963D

1.5A SWITCHING REGULATOR

- 1.5A OUTPUT LOAD CURRENT
- 5.1 TO 36V OUTPUT VOLTAGE RANGE
- DISCONTINUOUS VARIABLE FREQUENCY MODE
- PRECISE (+/–2%) ON CHIP REFERENCE
- VERY HIGH EFFICIENCY
- VERY FEW EXTERNAL COMPONENTS
- NO FREQ. COMPENSATION REQUIRED
- RESET AND POWER FAIL OUTPUT FOR MICROPROCESSOR
- INTERNAL CURRENT LIMITING
- THERMAL SHUTDOWN



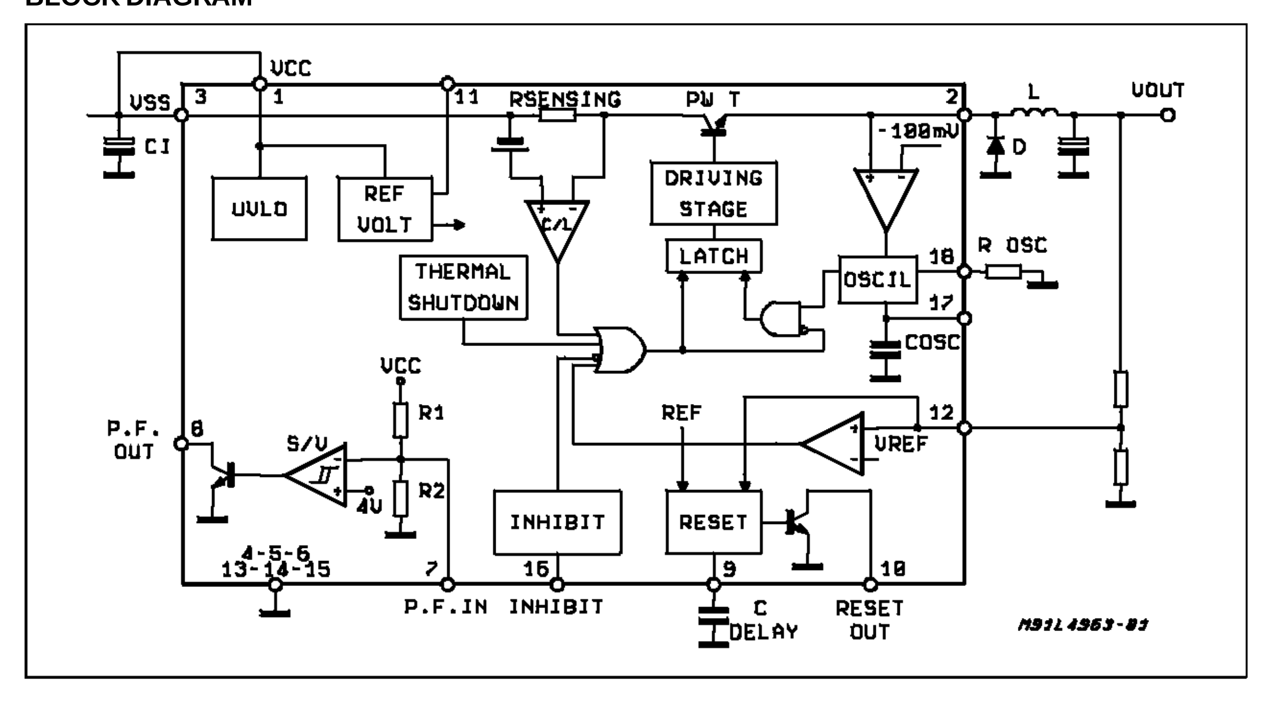


DESCRIPTION

The L4963 is a monolithic power switching regulator delivering 1.5A at 5.1V. The output voltage is adjustable from 5.1V to 36V, working in discontinuous variable frequency mode. Features of the device include remote inhibit, internal current limiting and thermal protection, reset and power fail outputs for microprocessor.

The L4963 is mounted in a 12+3+3 lead Powerdip (L4963) and SO20 large (L4963D) plastic packages and requires very few external components.

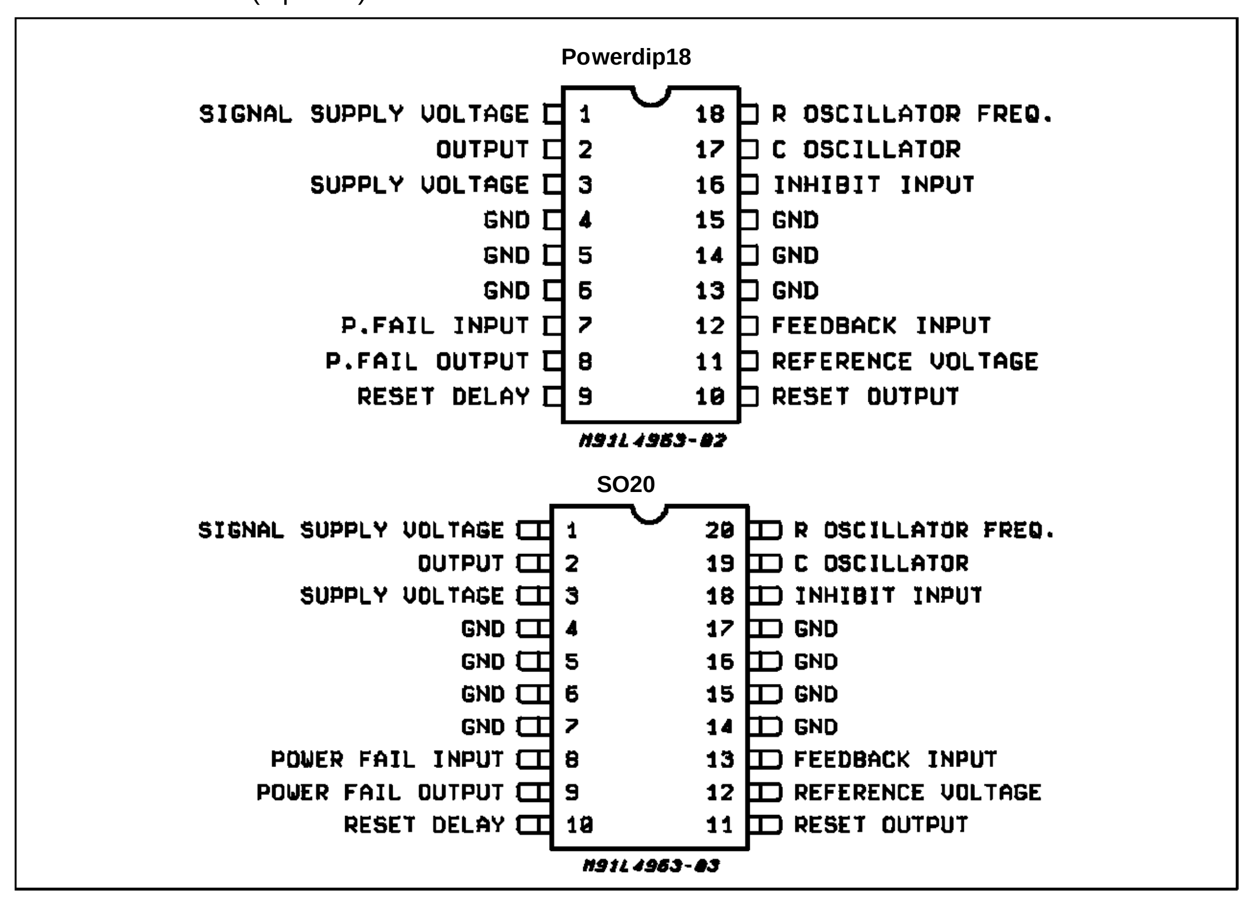
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol		Parameter	Value	Unit
SO20	Powerdip			
V_i		Input Voltage (pin 1 and pin 3 connected togheter)	47	V
V_3–V_2		Input to Output Voltage Difference	47	V
V_2		Negative Output DC Voltage	–1	V
V_2		Negative Output Peak Voltage at t=0.2 µs, f=50kHz	–5	V
V_8	V_7	Power Fail Input	25	V
V_9, V_{11}	V_8, V_{10}	Reset and Power Fail Output	V_i	
V_{10}	V_9	Reset Delay Input	5.5	V
V_{13}, V_{18}	V_{12}, V_{16}	Feedback and Inhibit Inputs	7	V
V_{19}, V_{20}	V_{17}, V_{18}	Oscillator Inputs	5.5	V
P_{tot}		Total Power Dissipation Tpins ≤ 90°C (Power DIP) (T_{amb} = 70°C no copper area on PCB) (T_{amb} = 70°C, 4cm^2 copper area on PCB)	5 1.3 2	W W W
T_{stg}, T_j		Storage & Junction Temperature (Tamb = 70°C 6cm^2 copper area on PCB)	–40 to 150 1.45	°C W
P_{tot}		Total Power Dissipation Tpins ≤90°C (SO20L)	4	W

PIN CONNECTION (top view)





PIN FUNCTIONS

SO20L	Power DIP	Name	Description
1	1	SIGNAL SUPPLY VOLTAGE	Must be Connected to pin 3
2	2	OUTPUT	Regulator output
3	3	SUPPLY VOLTAGE	Unregulated voltage input. An internal regulator powers the internal logic.
4, 5, 6, 7 14, 15, 16, 17	4, 5, 6 13, 14, 15	GROUND	Common ground terminal
8	7	POWER FAIL INPUT	Input of the power fail circuit. The threshold can be modified introducing an external voltage divider between the Supply Voltage and GND.
9	8	POWER FAIL OUTPUT	Open collector power fail signal output. This output is high when the supply voltage is safe.
10	9	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
11	10	RESET OUTPUT	Open collector reset signal output. This output is high when the output voltage value is correct.
12	11	REFERENCE VOLTAGE	Reference voltage output.
13	12	FEEDBACK INPUT	Feedback terminal of the regulation loop. The output is connected directly to this terminal for 5.1V operation; it is connected via a divider for higher voltages.
18	16	INHIBIT INPUT	TTL level remote inhibit. A logic low level on this input disables the device.
19	17	C OSCILLATOR	Oscillator waveform. A capacitor connected between this terminal and ground modifies the maximum oscillator frequency.
20	18	R OSCILLATOR FREQ.	A resistor connected between this terminal and ground defines the maximum switching frequency.

THERMAL DATA

Symbol	Parameter		SO20	Powerdip	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction to Pins	max.	15	12	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient (*)	max.	85	80	°C/W

(*) See Fig. 28



CIRCUIT DESCRIPTION (Refer to Block Diagram)

The L4963 is a monolithic stepdown regulator providing 1.5A at 5.1V working in discontinuous variable frequency mode. In normal operation the device resonates at a frequency depending primarily on the inductance value, the input and output voltage and the load current. The maximum switching however can be limited by an internal oscillator, which can be programmed by only one external resistor.

The fondamental regulation loop consists of two comparators, a precision 5.1V on-chip reference and a drive latch. Briefly the operation is as follows: when the choke ends its discharge the catch freewheeling recirculation filter diode begins to come out of forward conduction so the output voltage of the device approaches ground. When the output voltage reaches –0.1V the internal comparator sets the latch and the power stage is turned on. Then the inductor current rises linearly until the voltage sensed at the feedback input reaches the 5.1V reference.

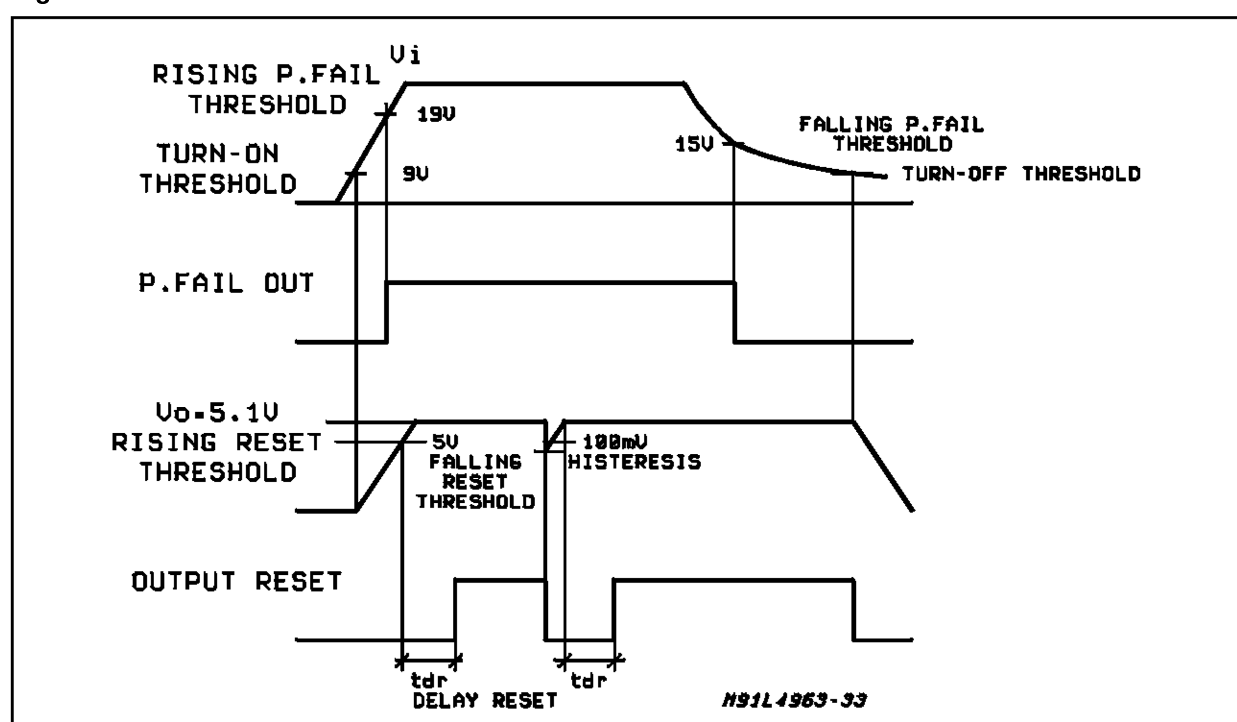
The second comparator then resets the latch and the output stage is turned off. The current in the choke falls linearly until it is fully discharged, then the cycle repeats. Closing the loop directly gives an output voltage of 5.1V. Higher output voltages are obtained by inserting a voltage divider and this method of control requires no frequency compensation network. At output voltages greater than 5.1V the available output current must be derated due to the increased power dissipation of the device.

Output overload protection is provided by an internal current limiter. The load current is sensed by a on-chip metal resistor connected to a comparator which resets the latch and turns off the power stage in overload condition. The reset circuits (see fig. 1) generates an output high signal when the output voltage value is correct. It has an open collector output and the output signal delay time can be programmed with an external capacitor. A powerfail circuit is also available and is used to monitor the supply voltage. Its output goes high when the supply voltage reaches a pre-programmed treshold set by a voltage divider to its input from the supply to ground. With the input left open the threshold is approximately equal to 5.1V. The output of the power fail is an open collector.

A TTL level inhibit is provided for applications such as remote on/off control. This input is activated by a low logic level and disables circuits operation.

The thermal overload circuit disables the device when the junction temperature is about 150°C and has hysteresis to prevent unstable conditions.

Figure 1: Reset and Power Fail Function



ELECTRICAL CHARACTERISTIC (Refer to the test circuit V_i = 30V T_j = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
DYNAMIC CHARACTERISTICS							
V_o	Output Voltage Range	V_i = 46V I_o = 0.5A	V_{ref}		36	V	2
V_i	Input Voltage Range	V_o = V_{ref} to 36V I_o = 0.5A	9		46	V	2
V_{12}	Feedback Voltage	V_i = 9 to 46V I_o = 0.5A	5	5.1	5.2	V	2
I_{12}	Input Bias Current	V_i = 15V V_{12} = 6V V_{17f} = 5V		5	20	µA	3a
V_{OS12}	Input Offset Voltage			5	10	mV	3a
ΔV_o	Line Regulation	V_i = 9 to 46V V_o = V_{ref} I_o = 0.5A		15	50	mV	2
ΔV_o	Load Regulation	V_o = V_{ref} I_o = 0.5 to 1.5A		15	45	mV	2
V_d	Dropout Voltage Between pin 3 and pin 2	I_2 = 3A V_i = 20V		1.5	2	V	2
I_{2L}	Current Limiting	V_i = 9 to 46V V_o = V_{ref} to 28V	3.5		6.5	A	2
I_o	Maximum Operating Load Current	V_i = 9 to 46V V_o = V_{ref}	1.5			A	2
SVR	Supply Voltage Ripple Rejection	V_i = 2Vrms V_o = V_{ref} fripple = 100Hz I_o = 1.5A	50	56		dB	2
V_{11}	Reference Voltage	V_i = 9 to 46V O < I_{11} < 5mA	5	5.1	5.2	V	3a
	Average Temperature Coefficient of Ref. Volt.	T_j = 0 to 125 °C		0.4		mV/°C	–
ΔV_{11}	V_{ref} Line Regulation	V_i = 9 to 46V		10	20	mV	3a
ΔV_{11}	V_{ref} Line Regulation	I_{ref} = 0 to 5mA V_i = 46V R_{osc} = 51KΩ	65 69	7	15	mV	3a
η	Efficiency	I_o = 1.5A V_o = V_{ref}	65	75		%	2
T_{sd}	Thermal Shutdown Junction Temperature		145	150		°C	–
	Hysteresis			30		°C	–
DC CHARACTERISTICS							
I_q	Quescent Drain Current	V_i = 46V I_o = 0mA; V_{16} = V_{12} = 0		14	20	mA	3a
		V_i = 46V I_o = 0mA; V_{16} = V_{ref} V_{12} = 5.3V		11	16	mA	3a
INHIBIT							
V_{16L}	Low Input Voltage	V_i = 9 to 46V	0.3		0.8	V	2
V_{16H}	High Input Voltage	V_i = 9 to 46V	2		5.5	V	2
I_{16L}	Input Current with Low Input Voltage	V_{16} = 0.8V		50	100	µA	2
I_{16L}	Input Current with High Input Voltage	V_{16} = 2V		10	20	µA	2

ELECTRICAL CHARACTERISTIC (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
RESET							
V_{12}	Rising Threshold Voltage	V_i = 9 to 46V	V_{ref} –150	V_{ref} –100	V_{ref} –50	mV	3b
V_{12}	Falling Threshold Voltage	V_i = 9 to 46V	V_{ref} –150	V_{ref} –200	V_{ref} –250	mV	3b
V_{9D}	Delay Rising Thereshold Voltage	V_7 = OPEN	4.3	4.5	4.7	V	3b
V_{9F}	Delay Falling Thereshold Voltage		1	1.5	2	V	3b
$-I_{9SO}$	Delay Source Current	V_9 = 4.7V V_{12} = 5.3V	70	110	140	µA	3b
I_{9SI}	Delay Sink Current	V_9 = 4.7V V_{12} = 4.7V	10			mA	3b
I_{10}	Output Leakage Current	V_i = 46V V_7 = 8.5V	50			µA	3b
V_{10}	Output Saturation Volt.	I_{10} = 15mA; V_I = 3 to 46V			0.4	V	3b
POWER FAIL							
V_R	Rising Threshold Voltage	Pin7 = open	17.5	19	20.5	V	3C
V_F	Falling Threshold Voltage	Pin7 = open	14.25	15	15.75	V	3c
V_7	Rising Threshold Voltage	V_i = 20V	4.14	4.5	4.86	V	–
V_7	Falling Threshold Voltage	V_i = 20V	3.325	3.5	3.675	V	–
V_s	Output Saturation Volt.	I_a = 5mA			0.4	V	3c
I_s	Output Leakage Current	V_i = 46V			50	µA	3c
OSCILLATOR							
f	Oscillator Frequency	R_T = 51KΩ	46	60	79	kHz	–
f	Oscillator Frequency	V_I = 9 to 46V T_j = 0 to 125°C R_T = 51KΩ	42		83	kHz	–

Figure 2: Test Circuit

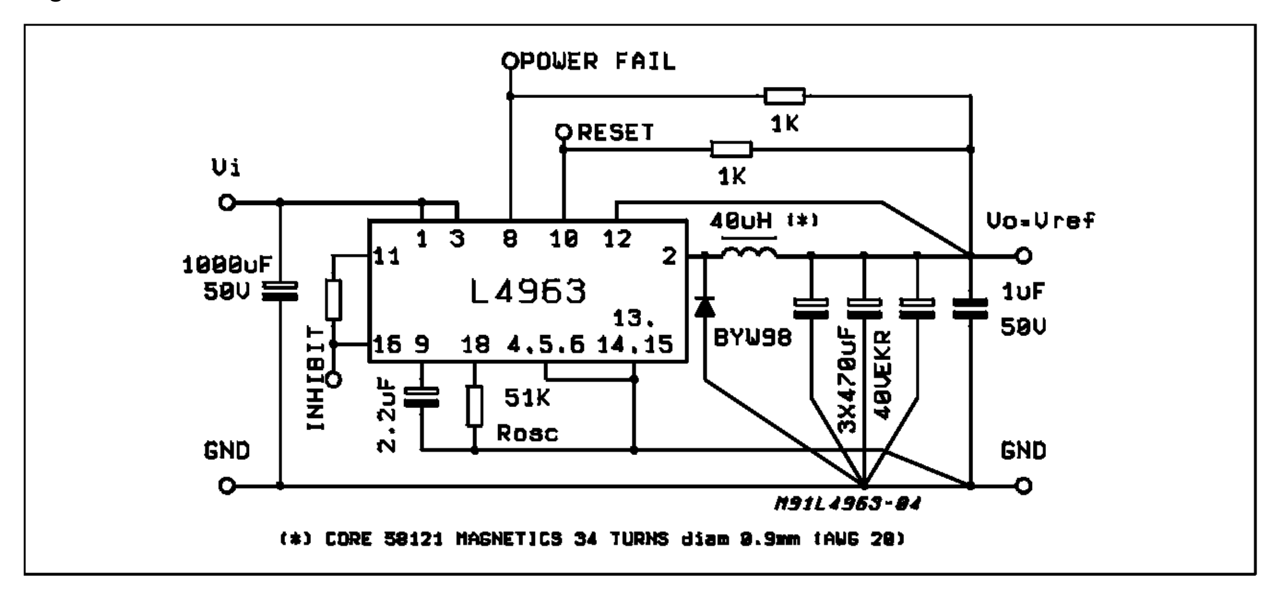


Figure 3: DC Test Circuit

Figure 3a

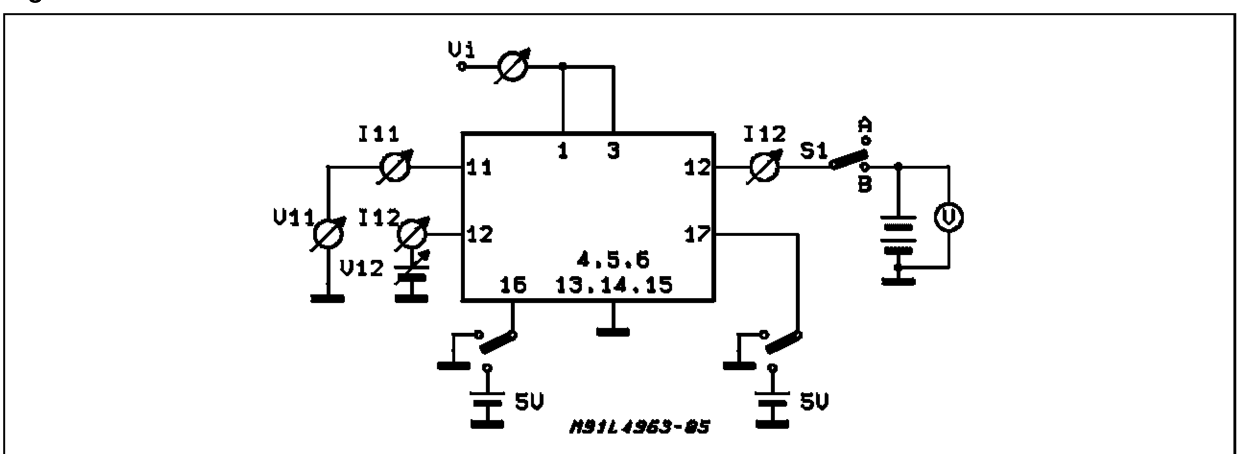


Figure 3b

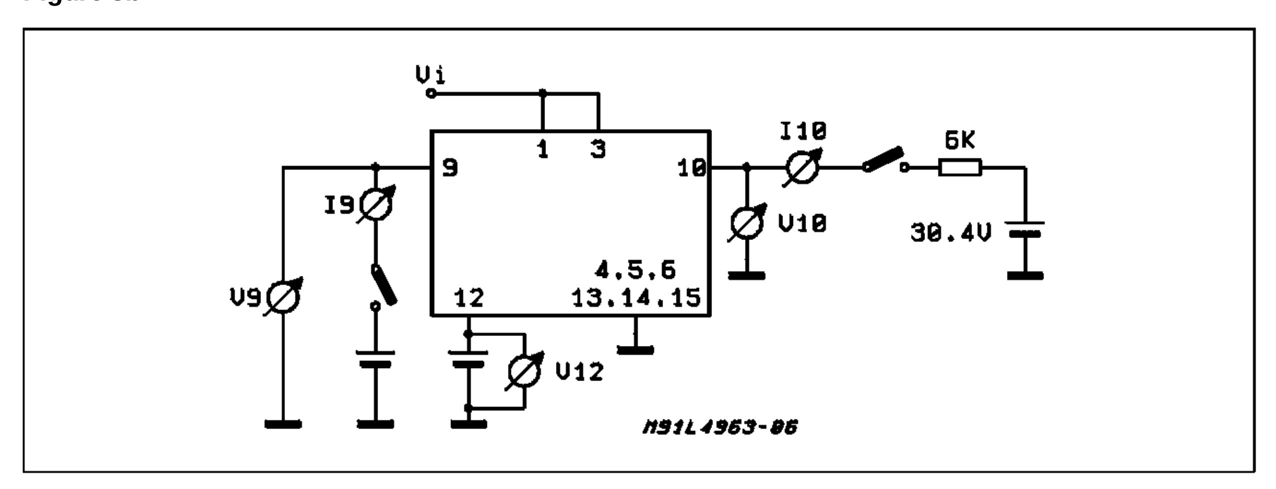


Figure 3c

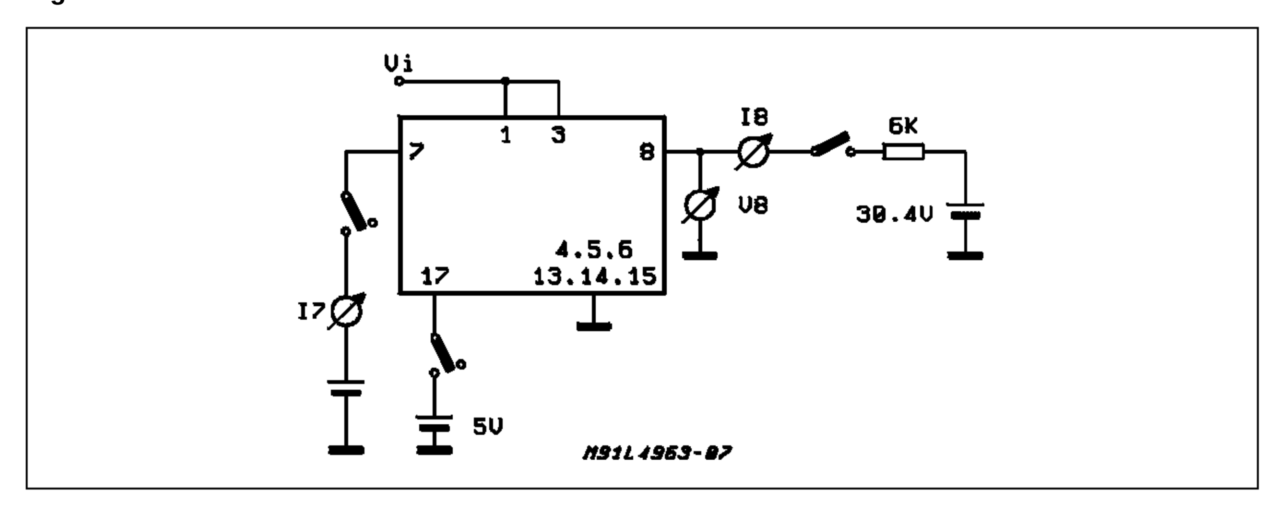


Figure 4: Quiescent Drain Current vs. Supply Voltage (0% Duty Cycle)

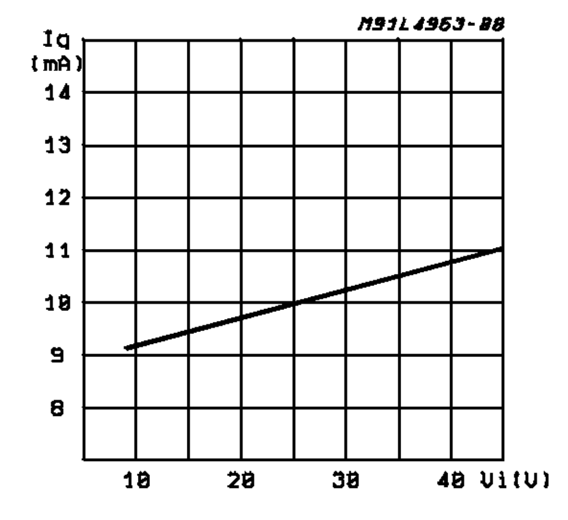


Figure 5: Quiescent Drain Current vs. Supply Voltage (100% Duty Cycle)

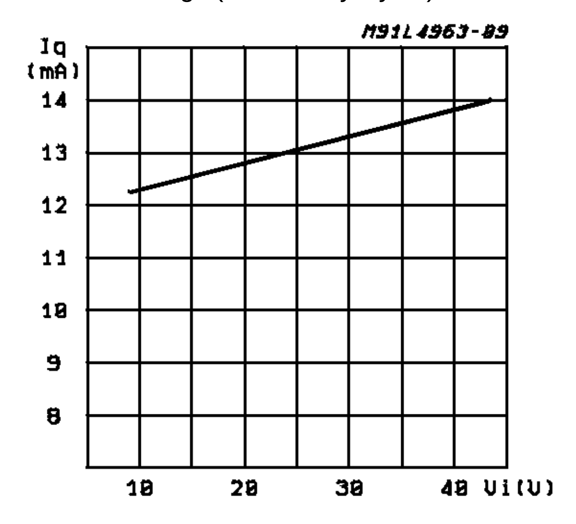


Figure 6: Quiescent Drain Current vs. Junction Temperature (0% Duty Cycle)

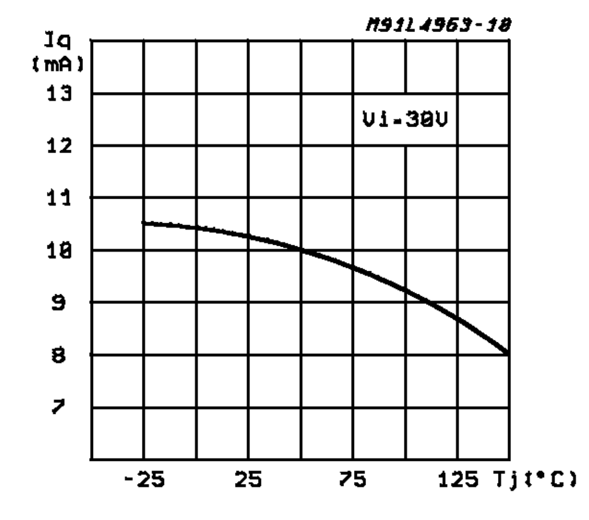


Figure 7: Quiescent Drain Current vs. Junction Temperature (100% Duty Cycle)

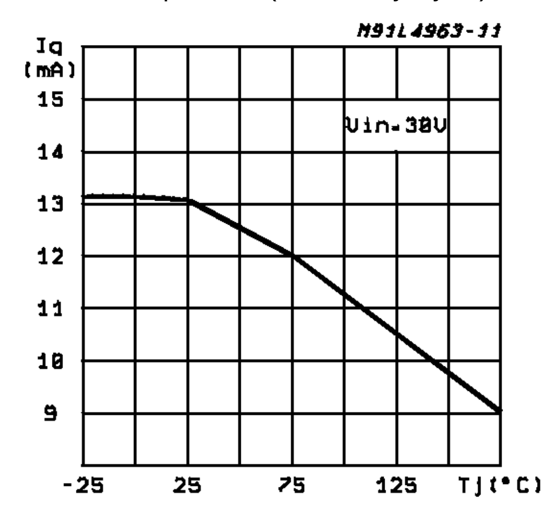


Figure 8: Reference Voltage vs. V_i

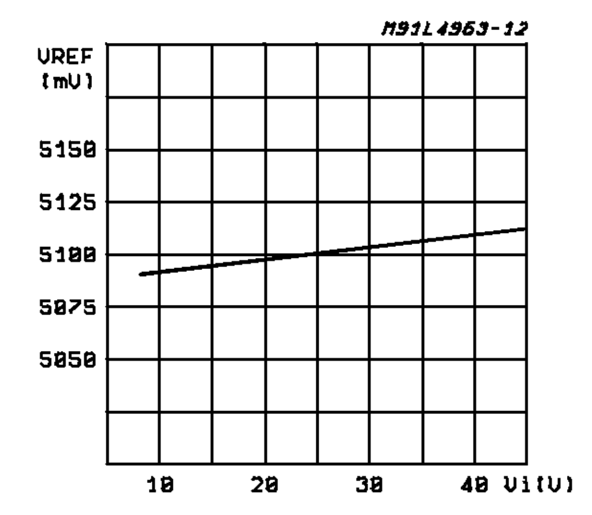


Figure 9: Reference Voltage vs. T_j

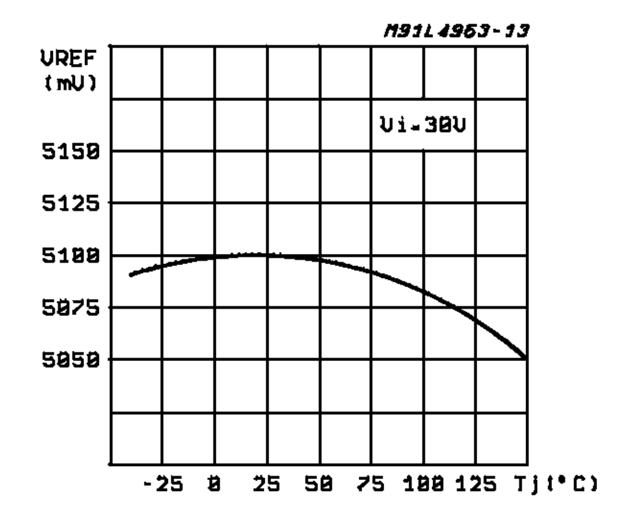


Figure 10: Line Transient Response

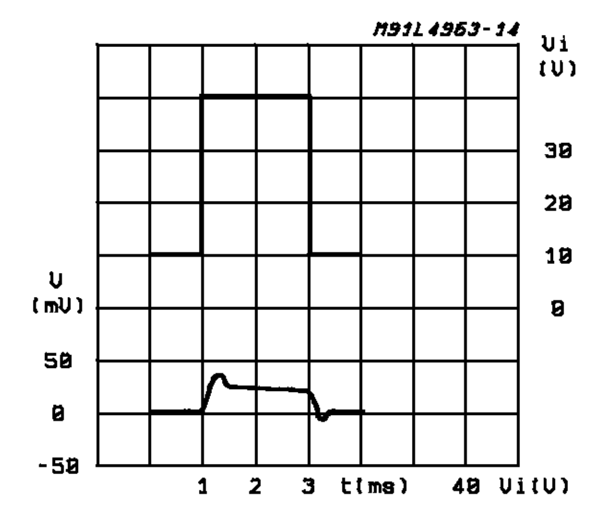


Figure 11: Load Transient

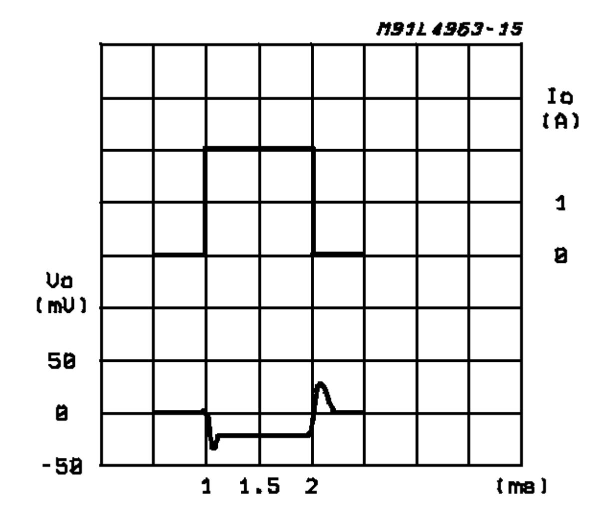


Figure 12: Supply Voltage Ripple Rejection vs. Frequency

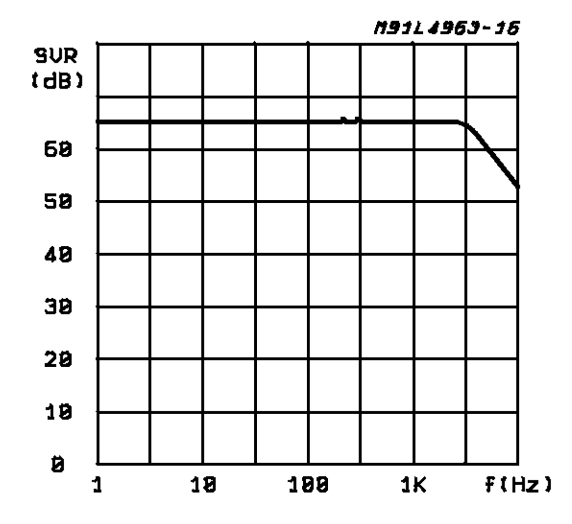


Figure 13: Dropout Voltage Between pi3 and 2 vs. Current at pin2

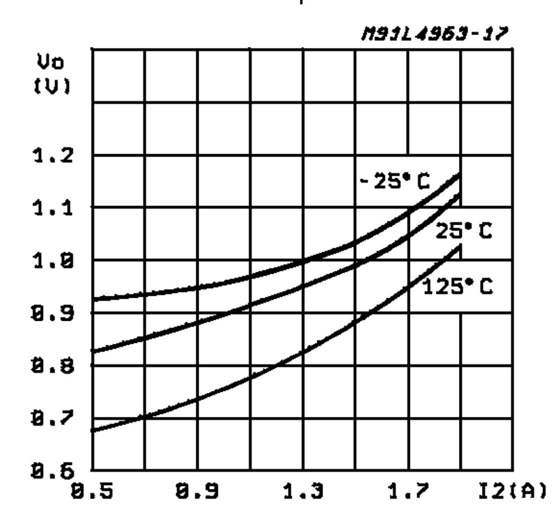


Figure 14: Dropout Voltage Between pin3 and 2 vs. Junction Temperature

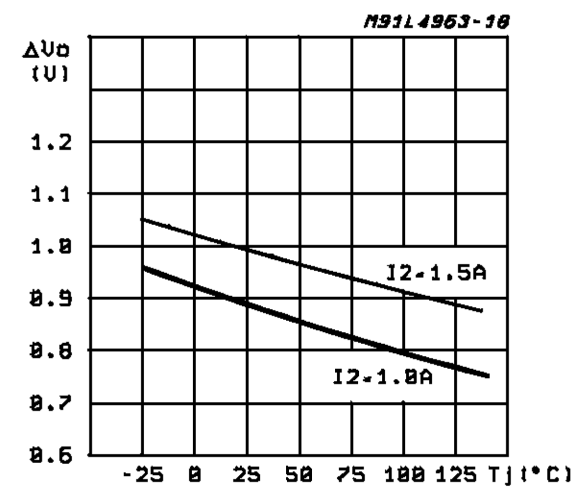


Figure 15: Maximum Allowable PowerDissipation vs. Ambient Temperature (Powerdip Package Only)

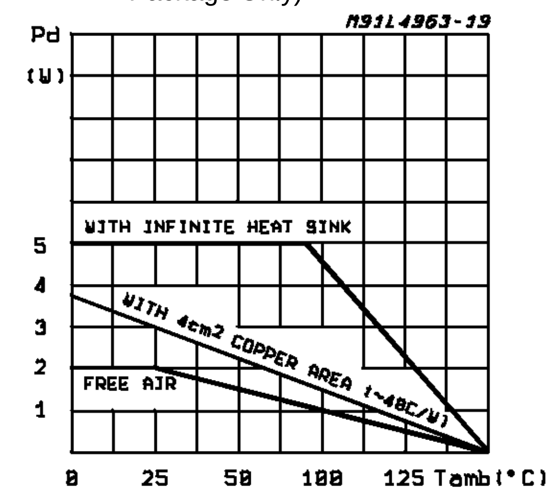


Figure 16: Power Dissipation (device only) vs. Input Voltage (Powerdip Package Only)

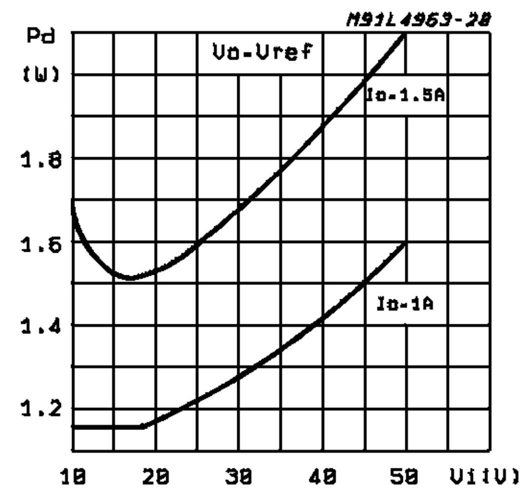


Figure 17: Power Dissipation (device only) vs. Output Voltage (Powerdip Package Only)

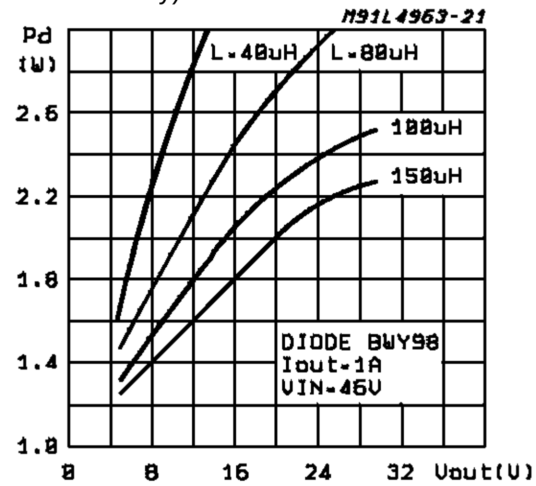


Figure 18: Voltage and Current Waveform at pin2

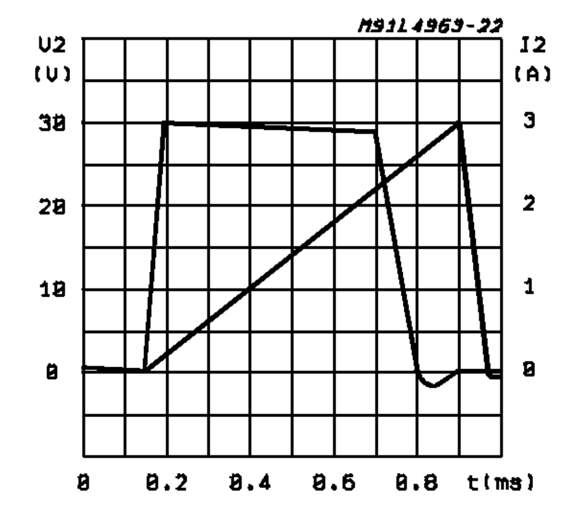


Figure 19: Efficiency vs. Output Current (Powerdip Package Only)

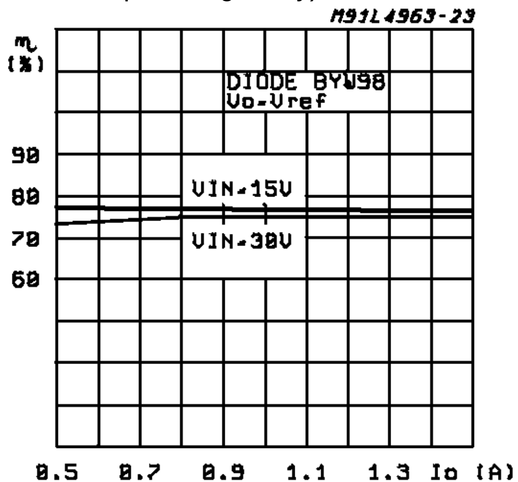


Figure 20: Efficiency vs. Output Voltage (Power-dip Package Only)

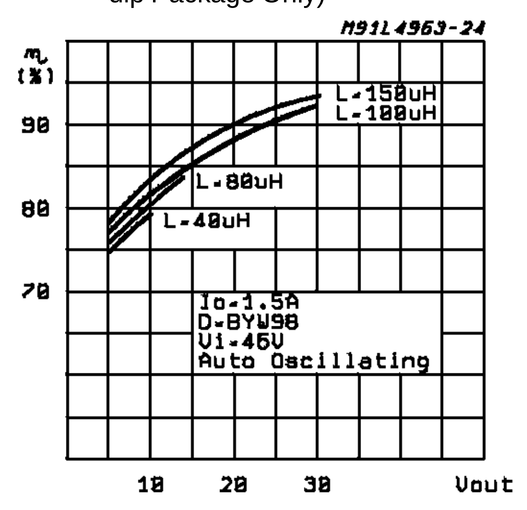


Figure 21: Current Limit vs. Junction Temperature V_i = 30V

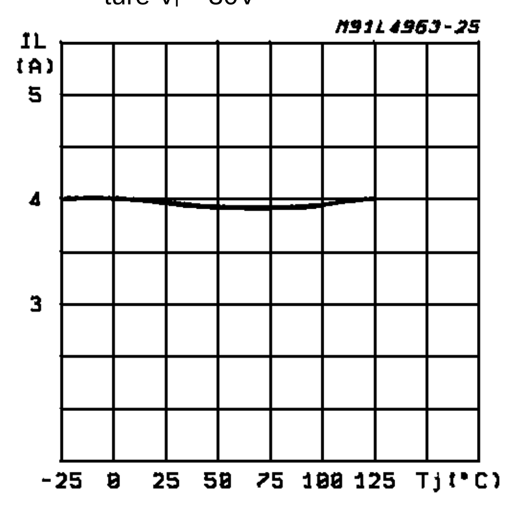


Figure 22: Current Limit vs. Input Voltage

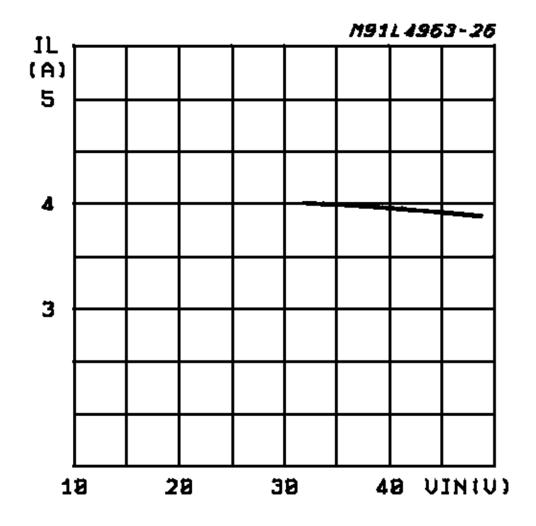


Figure 23: Oscillator Frequency vs. R2 (see fig. 26)

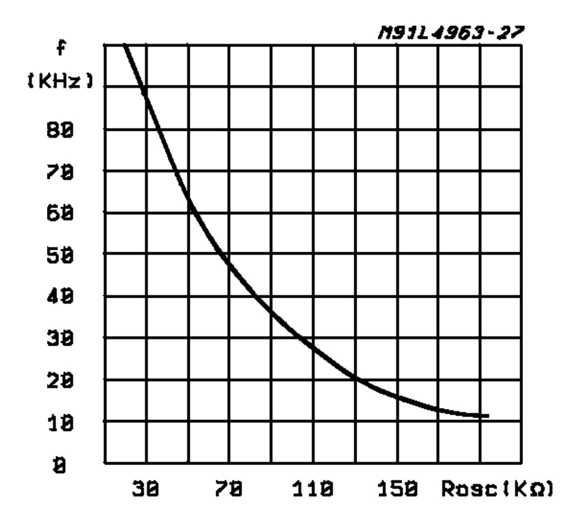


Figure 24: Oscillator Frequency vs. Junction Temperature

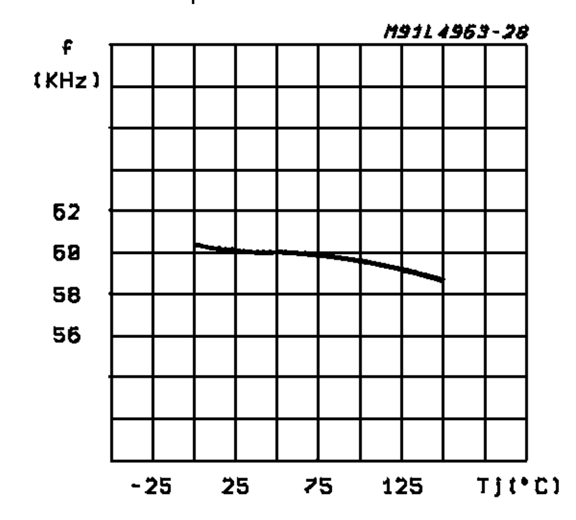


Figure 25: Oscillator Frequency vs. Input Voltage

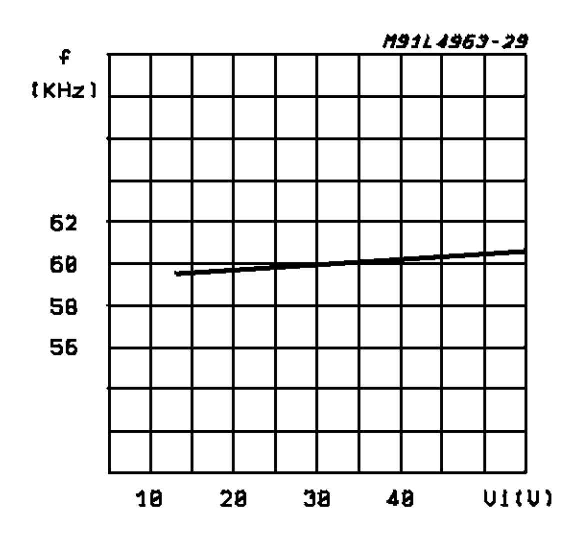
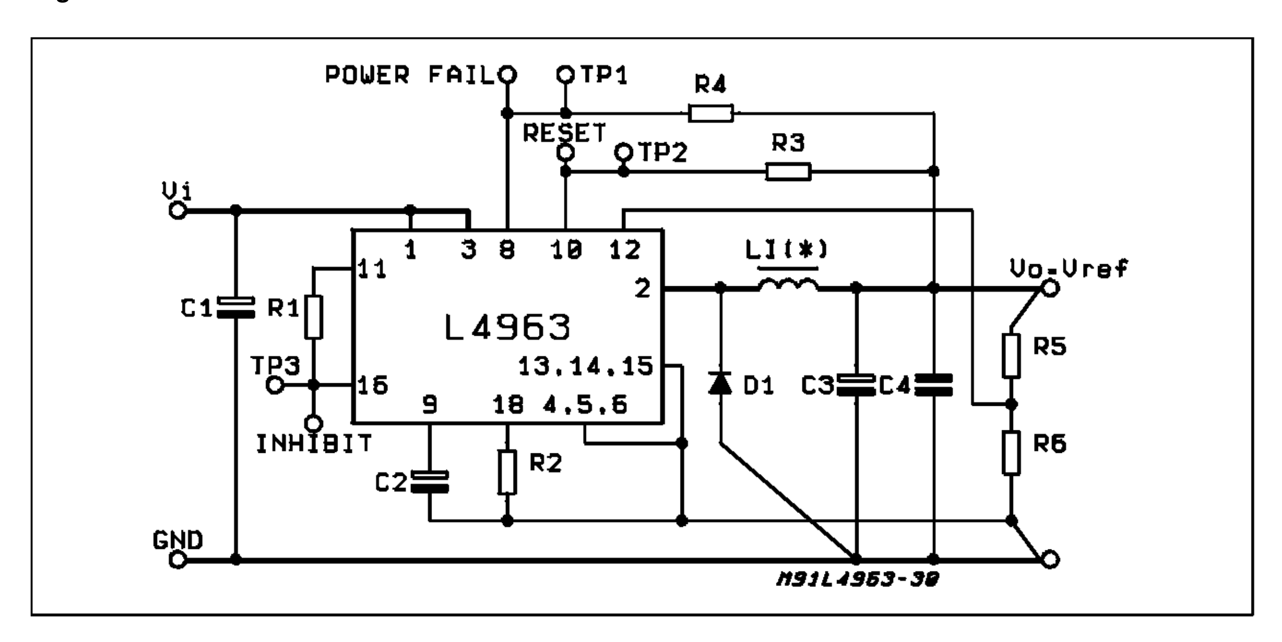


Figure 26: Evaluation Board Circuit



PART LIST

CAPACITOR	
C1	1000µF 50V EKR (*)
C2	2.2mF 16V
C3	1000µF 40V with low ESR
C4	1µF 50V film
RESISTOR	
R1	1KΩ
R2	51KΩ
R3	1KΩ
R4	1KΩ
R5, R6	see table

Resistor Values for Standard Output Voltages		
V_O	R6	R5
12	4.7KΩ	6.2KΩ
15	4.7KΩ	9.1KW
18	4.7KΩ	12KW
24	4.7KΩ	18KW

Diode: BYW98
Core: L = 40µH Magnetics 58121-A2MPP 34 Turns 0.9mm (20AWG)

(*) Minimum 100µF if V_i is a preregulated offline SMPS output or 1000µF if a 50Hz transformer plus rectifiers is used.

Figure 27: P.C. Board and Component Layout of the Circuit of fig. 26 (Powerdip Package) (1:1 scale).

Figure 28: Thermal Characteristics

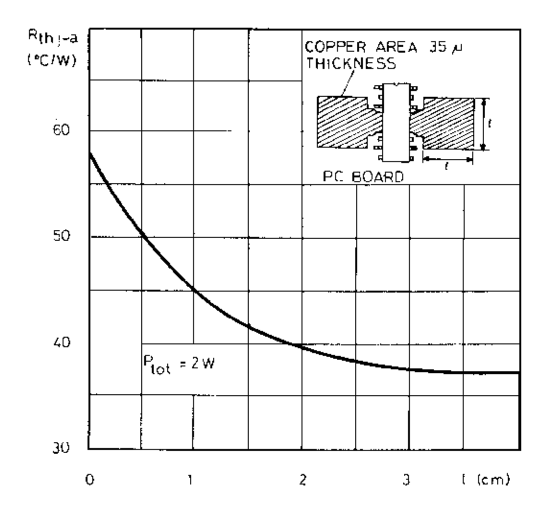


Figure 29: Junction to Ambient Thermal Resistance vs. Area on Board Heatsink (SO20)

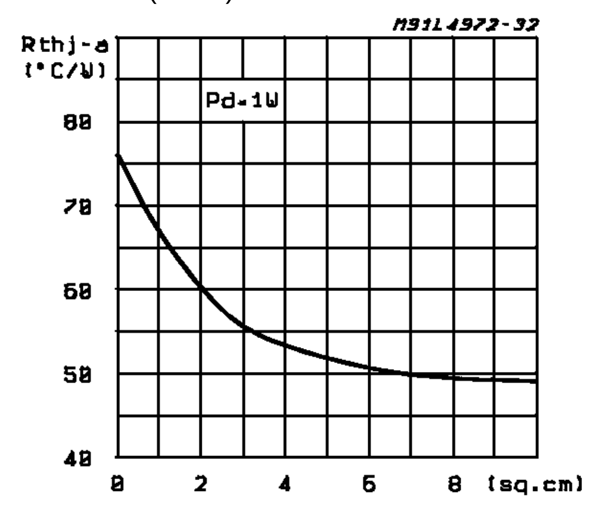


Figure 30: A Minimal 5.1 Fixed Regulator — Very Few Components are Required

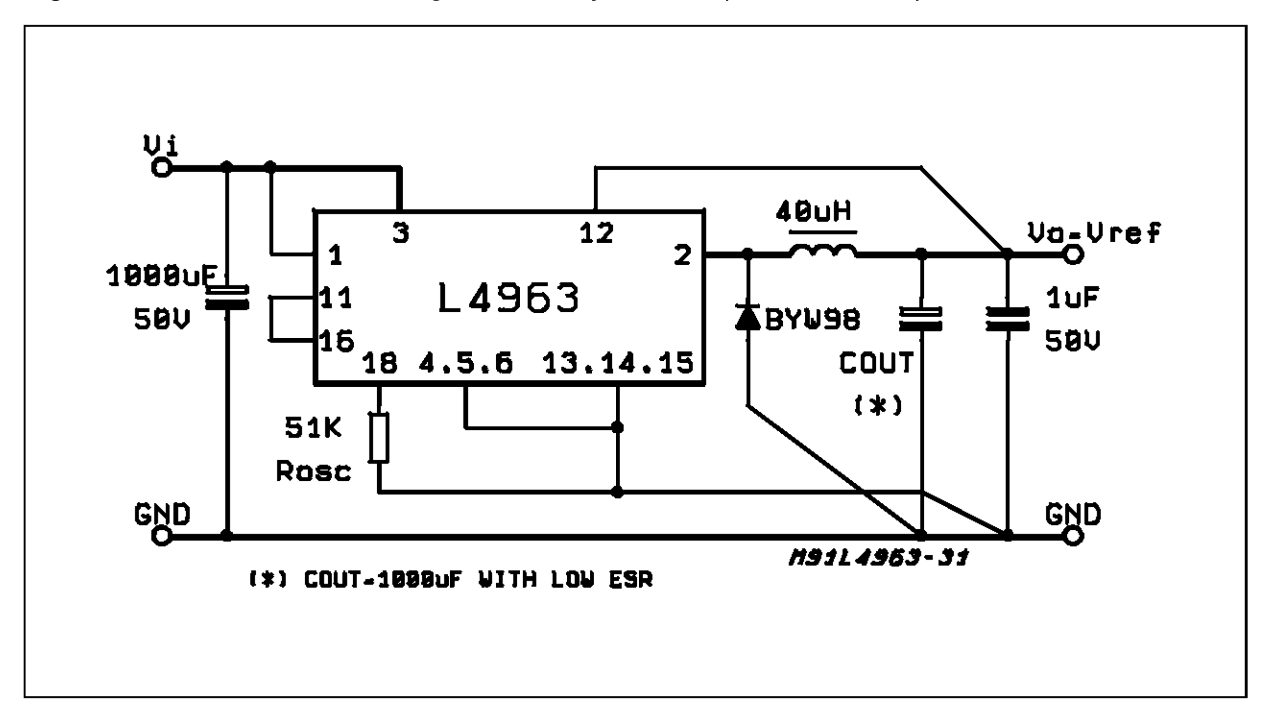
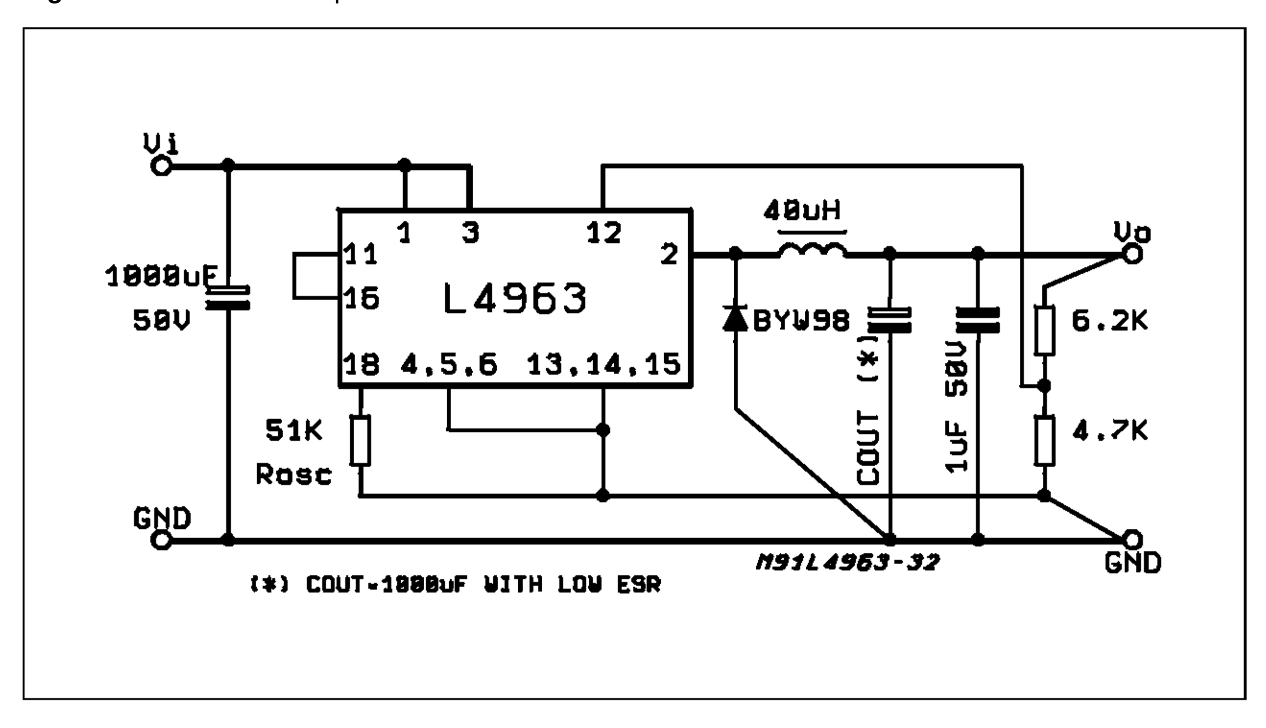
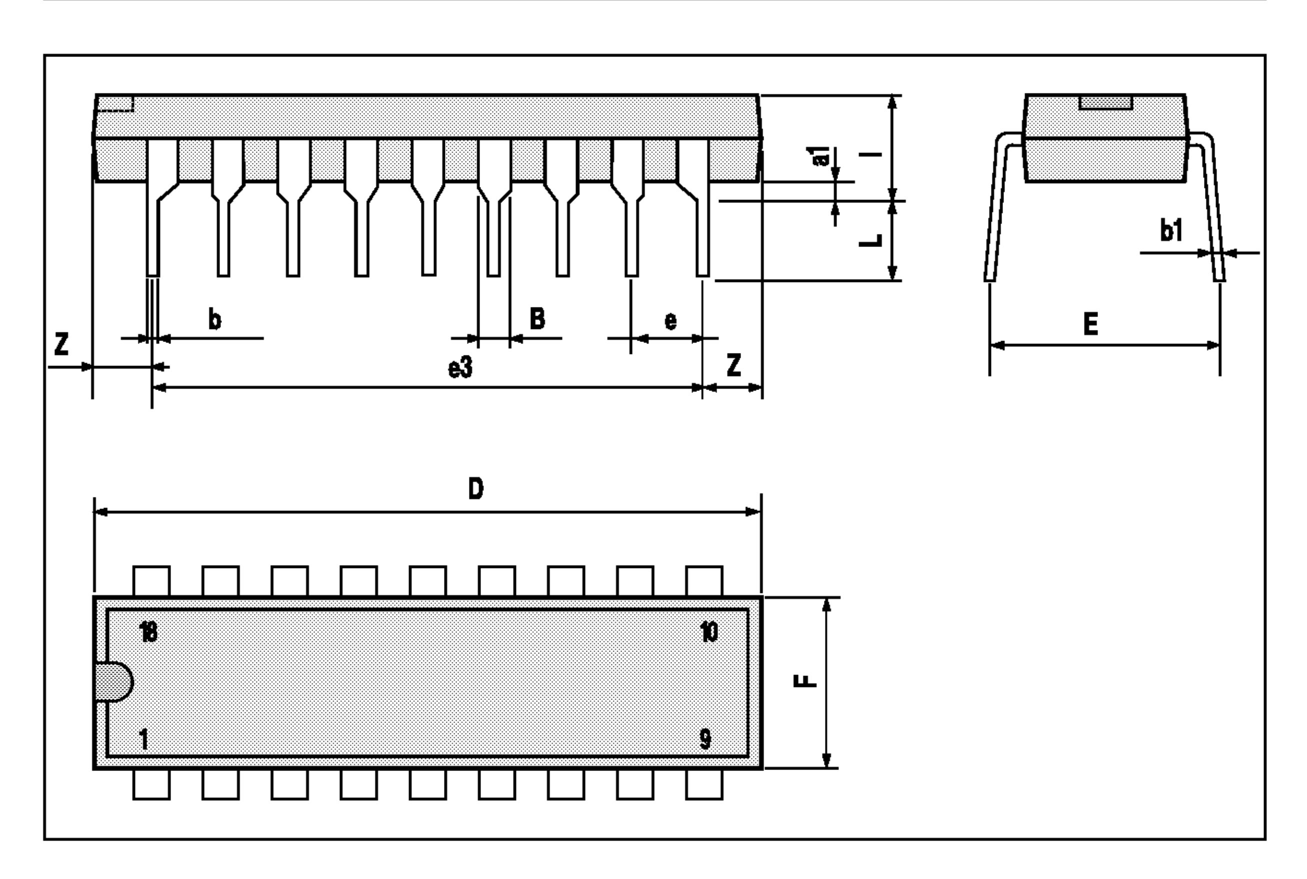


Figure 31: A Minimal Components count for V_O = 12V



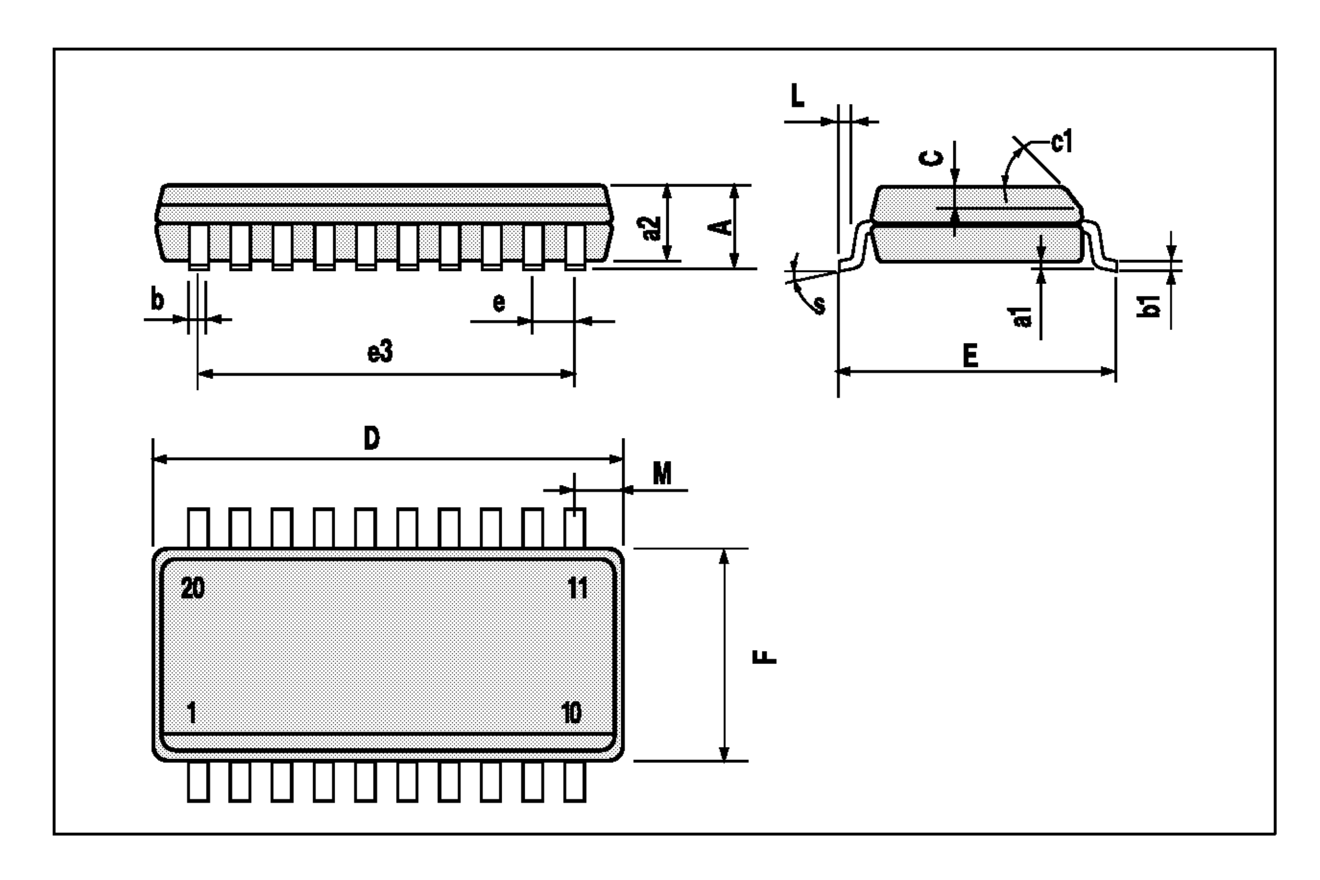
POWERDIP18 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			24.80			0.976
E		8.80			0.346	
e		2.54			0.100	
e3		20.32			0.800	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			2.54			0.100



SO20 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.3	0.004		0.012
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45 (typ.)					
D	12.6		13.0	0.496		0.512
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.299
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8 (max.)					




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